

METHOD AND PROGRAM PRODUCT OF LEVEL CONVERTER OPTIMIZATION

ABSTRACT OF THE INVENTION

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A method and program product for optimizing level converter placement in a multi supply integrated circuit. Each level converter is placed at a minimum power point to minimize net power and transitional delay from a first (low) voltage net source through the level converter and to a second (higher) voltage net sink. Then, inefficient level
10 converters are eliminated. Level converters with fanin cones below a selected minimum cone size are deleted and low voltage sources to the deleted level converter reverted. Higher voltage level circuit elements receiving inputs from multiple level converters are replaced with equivalent low voltage circuit elements. Low voltage buffer driving level converters are both replaced by a single said level converter.